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APPLICATION PAPERS

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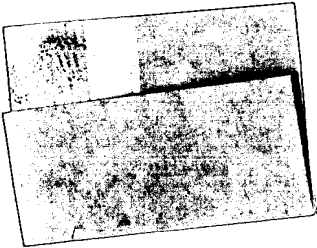20

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FOR

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DATA PROCESSING SYSTEM TRACE BUS

BACKGROUND OF THE INVENTION

Field of the Invention

5   This invention relates to the field of data processing systems.   More particularly, this invention relates to data processing systems including one or more trace data sources operable to generate individual trace data streams for diagnostic purposes.

10   ### Description of the Prior Art

It is known to provide data processing systems with trace data generating mechanisms.   Examples of such systems are the Embedded Trace Macrocells provided by ARM Limited of Cambridge, England.   Such trace mechanisms serve to monitor the data processing operations taking place and generate a trace data stream

15   indicative of the data processing operations occurring, such as which instructions are being executed, which data values are being manipulated.   This trace data stream is then output (possibly after on-chip buffering) to a diagnostic tool to assist a designer/programmer in debugging the system.

20   As data processing systems increase in complexity it is becoming common to use system-on-chip designs which typically contain many different data processing elements each performing its own data processing operations and communicating with the other data processing elements.   As an example, a single integrated circuit may include a processor core, a digital signal processor and a memory system.   Each of

25   these elements can be separately subject to tracing and generate its own trace data stream.   A problem with providing separate trace mechanisms for each trace data source is that separate inputs and outputs need to be provided for each trace data source in a manner that disadvantageously consumes pin count.   Furthermore, the different trace data output formats of some protocols that are appropriate and/or

30   necessary for some data processing elements can present a difficulty in a combined   ·
data stream.

It is known to provide trace systems which include trace source identifiers within the trace data protocol. This approach requires reading/unpacking of the data to determine trace data source.

5   **SUMMARY OF THE INVENTION**

Viewed from one aspect the present invention provides apparatus for processing data, said apparatus comprising:

at least one trace data source operable to generate an individual trace data stream including trace data signals and trace source identifying signals; and

10   a trace bus coupled to said at least one trace data source and including trace data signal lines operable to carry trace data signals and trace source identifying signal lines operable to carry trace source identifying signals.

The present technique recognises the need to combine trace data streams from

15   different sources and also the desirability of providing a system which is able to cope with a variety of different trace data sources without imposing undue constraints upon their form or operation. More particularly, the present technique recognises that separately providing data signal lines for carrying trace data signals and trace source identifying signal lines for carrying trace source identifying signals on a trace bus

20   yields a system which is able to deal with multiple trace data sources in a manner that imposes a low level of operational constraints on those trace data sources and yet preserves the flexibility to manipulate the trace data streams simply and effectively based upon trace source identifying signals.

25   In preferred embodiments of the invention the trace bus also includes one or more data size indicating signal lines operable to carry one or more size indicating signals. In this way, such preferred embodiments are able to utilise different data widths for the trace data signals with a common trace data bus and yet preserve efficiency when this trace data is to be stored or output off-chip by providing

30   associated size data that may be used in compaction processing.

Whilst it will be appreciated that the trace bus mentioned above could be used with a single data source, it is strongly advantageous in systems including a plurality of trace data sources and using a trace data stream combiner to combine trace data

streams. In these systems, respective trace data buses may couple the trace data sources to the trace data stream combiner which itself then produces a combined trace data stream using the same trace bus protocol. The trace bus of the present technique is particularly well suited to such a hierarchical approach using multiple trace data streams and in particular further trace data streams may be combined into a combined data stream at a later point if desired.

Preferred embodiments of the invention also provide a trace data stream replicator for replicating a single trace data stream into a plurality of trace data streams. These may then be subject to different post-replication processing, such as forming a low-bandwidth stream for immediate output and a high-bandwidth stream for on-chip buffering.

One technique which is highly useful and that is enabled by the provision of trace source identifying signals on the trace bus is the ability to filter the trace data streams in dependence upon the trace source identifying signals. Some trace data sources may be ignored or captured at low bandwidth whilst others may be captured at high bandwidth.

It will be appreciated by those familiar with the field that the identification of header data within a trace data stream is a common requirement in interpreting a trace data stream and can pose considerable practical difficulties. The present technique allows for a system in which a change in trace source identifying signals occurs whenever the trace data changes its source and accordingly header data may be inserted in the trace data stream at a fixed position relative to that change in trace source identifying signals. This simplifies subsequent interpretation of that trace data stream.

it will be appreciated that the trace data sources can take a wide variety of different forms and may be considered to include the processing elements which they are monitoring, such as a processor core, a digital signal processor and a memory bus monitor. A further preferred trace data source is one which may be software controlled, such as one which generates trace data in response to a software controlled write to one or more predetermined memory locations.

Whilst the present invention could be used in an apparatus composed of separately formed circuit elements, it is particularly well suited to embodiments in the form of an integrated circuit, such as a system-on-chip design.

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In order to positively and efficiently control the transfer of data via the trace bus preferred embodiments utilise a valid signal line which is indicative of a trace data source being active and generating trace data signals. The trace bus also advantageously includes a receiver ready signal line indicative of a trace data receiver

10 being active to receive trace data signals. The combination of the valid signal line and the receiver read signal line enables arbitration to be performed between different trace data sources which may simultaneously seek to generate trace data streams.

Viewed from another aspect the present invention provides a method of

15 processing data, said method comprising the steps of:

generating at least one individual trace data stream including trace data signals and trace source identifying signals using a respective trace data source;

carrying trace data signals upon trace data signal lines of a trace data bus; and

carrying trace source identifying signals upon trace source identifying signal

20 lines of said trace bus.

The above, and other objects, features and advantages of this invention will be apparent from the following detailed description of illustrative embodiments which is to be read in connection with the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 schematically illustrates an integrated circuit including multiple trace data sources;

30   Figure 2 schematically illustrates a trace data replicator;

Figure 3 illustrates a trace data bus;

Figure 4 illustrates the interaction between a valid signal, a data signal and a ready signal; and

Figure 5 schematically illustrates the relationship between a change in trace source identifying signal and the presence of header data within the trace data.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows an integrated circuit 2 in the form of a system-on-chip integrated circuit including a processor core 2, a digital signal processor 4, a memory 6 and a software controlled trace data source 8 all connected via a main bus 10, such as an AMBA bus as designed by ARM Limited, Cambridge, England. Associated with each of the data processing elements 2, 4, 6, 8 is a trace data generator 12, 14, 16, 18 which is responsive to events and conditions occurring within the data processing element which they are monitoring to generate a trace data stream. The type of events being monitored will be familiar to those in the trace field, such as the instructions being executed, the data values being manipulated, data values being read or written to particular memory locations or the writing of a data value to a predetermined memory location serving as a trace output (e.g. the action of the software controlled trace generator is such that a data value written to a location within a predetermined address range is output as trace data so as to allow software being executed to be instrumented to output diagnostic data in the form of trace information).

The trace data streams that have been generated are output on a respective trace bus 20, 24 to a respective trace data stream combiner 22, 26. Each of the trace data sources 12, 14, 16, 18 is provided with a trace data bus and the associated trace data stream combiner 22, 26 acts as a multiplexer. The output of the trace data stream combiner 22, 26 is also in the form of a trace bus having the same signals.

As will be seen in Figure 1, the trace data streams may be hierarchically combined, i.e. the first trace data stream combiner 22 combines the trace data streams from the trace sources 12, 14, 16 and the second trace data stream combiner 26 combines the trace data stream output from the first trace data stream combiner 22 with that output from the software controlled trace data generator 18.

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A trace data stream replicator 28 serves to replicate the trace data stream output from the trace data combiner 26 into two initially identical trace data streams that are fed through different channels. The first of these trace data streams serves as

5   a low-bandwidth output which is passed through a formatter 30 and a trace port interface unit 32 before being output off-chip in real time. A second of the trace data streams output from the trace data stream replicator 28 is output through a formatter 34 and then stored within an on-chip embedded trace buffer memory 36. Since this data is kept on-chip, it may be a high-bandwidth signal capturing a higher level of

10   detail. It will be appreciated that the formatters 30, 34 serve to compress and compact the trace data stream present on the trace bus to have a more information dense form to preserve off-chip bandwidth and storage space within the embedded trace buffer memory 36. The techniques for compressing trace data will be familiar to those in the technical field and will not be described further herein.

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Figure 2 schematically illustrates the operation of the trace data stream replicator 28. This receives a single trace data stream $DATA_{in}$ and generates two identical output trace data streams $DATA_{out1}$ and $DATA_{out2}$. The timing of the generation of these signals is controlled by an exchange of $READY_n$ and VALID

20   signals as will be discussed later in relation to Figure 4.

Figure 3 schematically illustrates the trace data bus 20, 24 in more detail. The trace data bus 20, 24 includes a valid signal ATVALID which indicates that the trace data source is outputting valid trace data and a trace data source ID onto the trace bus

25   20, 24. A 32-bit trace data signal ATDATA is generated by the trace data source and output on the trace bus 20, 24 to the trace data receiver. A 7-bit trace data source identifying signal ATID is generated by the trace data source and output on the trace bus 20, 24 to the trace data receiver. The trace bus 20, 24 also includes trace data size identifying signals ATSIZE which are generated by the trace data source and received

30   by the trace data receiver and serve to indicate the data width upon the signals ATDATA. A two-bit size signal is provided and this may be used to specify how many bytes of the four bytes available on the 32-bit ATDATA portion of the trace bus 20, 24 are being used by the current trace data source. This size information is highly

useful for the formatters 30, 34 which subsequently compress, or at least reformat the trace data stream.

A trace data receiver ready single ATREADYnis generated by the trace data receiver and output to the trace data source. In the context of the embodiment of Figure 1, the trace data receiver may be either the trace data stream combiner 26 or the trace data stream combiner 22 or 28 (replicator), 32 (TPIU), 36 (ETB) whilst the trace signal sources may be any of the sources 12, 14, 16 and 18.

Figure 3 illustrates that the trace data signals ATDATA and the trace source identifying signals ATID are provided with their own dedicated signal lines on the trace bus 20, 24. The provision of the trace source identifying signals as a separate portion on the trace bus 20, 24 frees the protocol and format of the trace data itself ATDATA from having to have embedded within it trace source identifying signals for use within a multi-source environment. This provides an advantageously modular and scaleable structure for supporting multi-source tracing.

Another feature of the provision of the trace data source identifying signals is that selective filtering or other processing may be performed upon the trace data stream in dependence upon the trace source data identifying signals. Thus, the formatters 30, 34 of Figure 1 may selectively remove trace data associated with an "uninteresting" trace data source whilst maintaining trace data associated with a more critical trace data source in its full form. The trace data source identifying signals may be also used to insert appropriate trace data source identifying codes within a combined trace data output stream that is generated by the formatters 30, 34.

Figure 4 schematically illustrates the action of the valid and ready signals in controlling the sending of trace data from a trace data source to a trace data receiver. A first trace data word A is sent and is indicated as being asserted upon the trace bus 20, 24 by the ATVALID signal going high. Whilst the trace data word A is being output the ATREADYn signal is low indicating that the trace data receiver is ready to receive that trace data word and accordingly that trace data word is successfully captured. Sometime later the trace data source tries to output a second trace data word B. At this time the ready signal ATREADYn is high and so this trace data word

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is resent in the following cycle by which time the ready signal has gone low and the trace data word B is successfully captured. Thus, a trace data receiver can effectively arbitrate between multiple trace data sources. Techniques for arbitrating between trace data sources, alternatively described as bus masters, will be familiar to designers

5   of other system busses, for example a main bus 10. The trace data sources assume they will be able to send their trace data and assert it on their private trace bus to the trace data receiver. The trace data receiver indicates whether or not it was ready to receive that data using the ready signal. If the ready signal was not asserted when the trace data was sent, then the trace data source resends the trace data.

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Figure 5 schematically illustrates the relationship between trace data source identifying signals and header data within the trace data stream. As will be familiar to those in the tracing field header data is often inserted within a trace data stream to indicate parameters associated with the following trace data. This header data must

15   be correctly identified within the trace data stream in order that it can be distinguished from trace data itself and properly decoded to be used in the subsequent decoding of the trace data. The correct identification of header data within a trace data stream is a problem within the tracing field. The present technique provides a system wherein whenever the trace data source identifying signal changes, a data header is inserted

20   with a predetermined location relative to that change in trace data source identifying signal. In the example illustrated, the header is inserted at the point at which the trace data source identifying signal itself changes, although a fixed offset could be used instead. This simplifies subsequent processing of the trace data stream since by monitoring the trace source identifying signal for changes, header data can be

25   identified in the trace data and accordingly properly decoded.

Although illustrative embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and

30   modifications can be effected therein by one skilled in the art without departing from the scope and spirit of the invention as defined by the appended claims.